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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,604	08/30/2000	Thomas J. Krutsick	5	9105
7590	10/06/2003			
Lucent Technologies Inc Docket Administrator Rm 3C 512 PO Box 636 600 Mountain Avenue Murray Hill, NJ 07974-0636			EXAMINER SEFER, AHMED N	
			ART UNIT 2826	PAPER NUMBER

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/650,604

Applicant(s)

KRUTSICK, THOMAS J.

Examiner

A. Sefer

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 28-30 and 32-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-30 and 32-39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Response to Amendment***

1. The amendment filed on 7/22/03 has been entered; no new claims have been added.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 28-30, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo US Patent No. 4,609,935 in view of Nelson et al. USPN 3,683,491.

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body; a field plate 39 comprising polysilicon (as in claim 29) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; a second insulating layer 42, with a first portion of the second insulating covering the field plate, an electrical contact to the top surface of the field plate; an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate

by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window

Nelson et al disclose in fig. 9 a field plate 46 with a portion of the bottom surface extending through a contact window in an insulating layer 32 and into contact with a contact region 38 of a resistor 34.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching Nelson et al with Kondo's device, since that would provide high values of resistance.

As to claim 30, Kondo discloses first and second insulating oxide layers.

As to claims 33 and 34, Kondo discloses a barrier layer 41.

4. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Nelson et al. as applied to claims 28 and 29 above, and further in view of Davis et al. USPN 5,200,733.

The combined references disclose the device structure as recited in the claim, but do not disclose an insulative spacer formed around a field plate.

Davis et al disclose in fig. 11 an insulative spacer 40 around a field plate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulative spacer around a field plate, since that would provide the field plate an excellent insulation.

5. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo US Patent No. 4,609,935 in view of Nelson et al. USPN 3,683,491.

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body; a field plate 39 on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; a second insulating layer 42, with a first portion of the second insulating covering the field plate, a metal layer comprising an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window.

Nelson et al disclose in fig. 9 a field plate 46 with a portion of the bottom surface extending through a contact window in an insulating layer 32 and into contact with a contact region 38 of a resistor 34.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching Nelson et al with Kondo's device, since that would provide high values of resistance.

6. Claims 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo US Patent No. 4,609,935 in view of Nelson et al. USPN 3,683,491.

Kondo discloses (see figs. 4-10 and col. 6, lines 46-49) a method of the manufacture of an integrated circuit having a field-plated resistor, the field-plated resistor comprising forming a resistor body 35 in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; forming a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body; forming a field plate 39 comprising polysilicon (as in claim 37) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; depositing a second insulating layer 42, with a first portion of the second insulating covering the field plate; depositing a metal layer comprising an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window.

Nelson et al disclose in fig. 9 a field plate 46 with a portion of the bottom surface extending through a contact window in an insulating layer 32 and into contact with a contact region 38 of a resistor 34.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching Nelson et al with Kondo's device, since that would provide high values of resistance.

As to claim 38, Kondo discloses first and second insulating oxide layers.

7. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Nelson et al. as applied to claims 36 and 38 above, and further in view of Davis et al. USPN 5,200,733.

The combined references disclose the device structure as recited in the claim, but do not disclose an insulative spacer formed around a field plate.

Davis et al disclose in fig. 11 an insulative spacer 40 around a field plate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulative spacer around a field plate, since that would provide the field plate an excellent insulation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

NATHAN J. FLYNN  
SUPERVISOR OF PAT. EXAMINER  
TECHNICAL CENTER 2826

ANS  
September 28, 2003